UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/063,316	04/10/2002	Joseph A. Iadanza	BUR920010123	6885

23550 7590 08/04/2006

HOFFMAN WARNICK & D'ALESSANDRO, LLC
75 STATE STREET
14TH FLOOR
ALBANY, NY 12207

EXAMINER	
VLAHOS, SOPHIA	

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 08/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/063,316	IADANZA, JOSEPH A.	
	Examiner	Art Unit	
	SOPHIA VLAHOS	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-20* is/are rejected.

7)☒ Claim(s) *5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 April 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see "remarks" pages 9-10, filed 5/22/2006, with respect to the rejection(s) of (independent) claim(s) 1, 8, 15, and 18 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Cranford Jr. et. al. (U.S. 6,298,458).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-4, 6-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Cranford Jr. et, al. (U.S 6,298,458).

With respect to claim 1, Cranford et. al., disclose: a transmitter for receiving a network data signal representative of a signal capable of being transmitted over a network and a control signal for impairing characteristics of the network data signal (Fig. 5, see "transmitter side of BIST", data signal 221, and combination of elements control logic 220, and counters 215a, 215b, see column 3, lines 32-43, column 5, lines 23-37)

for continuously generating an output signal corresponding to the data signal and the control signal during a predetermined time window (see column 9, lines 4-21, test time window during which the test is run); a receiver for continuously receiving the output signal from the transmitter (Fig. 5, receive side of BIST, see column 3, lines 43-48), and for reconstructing the network data signal within the predetermined time window (see column 9, lines 4-21, column 10, lines 4-9); and a built-in-self-test (BIST) device for generating the network data signal and the control signal (Fig. 5, see column 3, lines 32-43) and for providing a clock signal with a varied offset for jitter testing the transceiver (column 8, lines 15-21, the clock source having high jitter is interpreted as the clock signal with a varied offset since jitter causes clock signal to have varied offsets (clock transitions/edges do not correspond (can be early and /or late) compared to ideal clock transitions), wherein the BIST device detects erroneous performance by the transceiver based on the reconstructed network data signal (column3, lines 45-47).

With respect to claim 2, all of the limitations of claim 2, are analyzed above in claim 1, and Cranford et. al. discloses: wherein the control signal includes signals for impairing a phase and an amplitude of the network data signal (see column 7, lines 65-67, column 8, lines 1-5, slurring control is understood to be relevant to an amplitude and phase impairment of the signal).

With respect to claim 3, all of the limitations of claim 3 are analyzed above in claim 1, and Cranford et. al., disclose: wherein the BIST device includes a jitter control system (see column 8, lines 18-21, the jitter selection control).

With respect to claim 4, all of the limitations of claim 4, are analyzed above in claim 3, and Cranford et. al., disclose: wherein the jitter control system varies an offset of a clock signal (see column 8, lines 18-21, the jitter selection control, understood that as a result of selecting a high jittered clock signal, the clock transitions are varied).

With respect to claim 6, all of the limitations of claim 6 are analyzed above in claim 1, and Cranford et. al., disclose: wherein the BIST device further comprises a pulse width counter for varying a pulse width of the network data signal (see column 5, lines 23-48, counters 215a and/or 215b , duty cycle (ratio of pulse duration over the period) corresponds to the pulse width).

With respect to claim 7, all of the limitations of claim 7 are analyzed above in claim 6, and Cranford et. al., disclose: wherein the pulse width counter tests a clock recovery capability of the receiver (column 5, lines 42-48 in understood that the pulse width counter is used to generate data that will test circuit responses, column 10, lines 12-17, where the recovered clock frequency may be compared to the expected clock frequency, i.e. the clock recovery capability of the receiver is tested).

With respect to claim 8 claim 8 is analyzed similarly to claim 1 above, and see column 8, lines 15-20, for using a test clock signal with high jitter, and the transmit side of Fig. 5, where the data is formulated based on the reference clock 210 and PLL clock recovery at the receiver (see Fig. 5, receiver side) implies that the clock is embedded in the data transmitted from the transmit side of the BIST.

With respect to claims 9, all of the limitations of claim 9, are analyzed above in claim 8, and Cranford et. al. discloses: wherein the control signal includes signals for impairing a phase and an amplitude of the network data signal (see column 7, lines 65-67, column 8, lines 1-5, slurring control is understood to be relevant to an amplitude and phase impairment of the signal).

With respect to claim 10, all of the limitations of claim 10 are analyzed above in claim 9, and Cranford et. al., disclose: wherein the BIST device comprises means for programming the network data signals (Fig.5, combination of counters 215a,215b and 220 control logic, as well as output signal 221 going to the protocol generator, see also column 4, lines 45-52 referring to the protocol generator in the transmitter side, and column 5, lines 26-27 i.e. the control logic allows programming of the network data).

With respect to claim 11, all of the limitations of claim 11, are analyzed above in claim 8, and Cranford et. al., disclose: wherein the transmitter and the receiver are provided on a single integrated circuit, the transceiver further comprising a transfer gate for selectively coupling the output signal from the transmitter to the receiver within the

integrated circuit (see Fig. 4, element 173, transfer gate).

With respect to claim 12, all of the limitations of claim 12 are analyzed above in claim 8, and Cranford et. al., discloses: wherein the network data signal includes an embedded clock signal, and wherein the BIST device comprises means for locking onto the embedded clock signal (see column 5, lines 58-62 , PLL clock recovery understood to recover an embedded clock signal from the received data signal).

With respect to claim 13, all of the limitations of claim 13 are analyzed above in claim 12 and Cranford et. al., disclose: wherein the means for detecting erroneous performance by the transceiver comprises a counter device for counting edge transitions of the clock signal for establishing a time window for reconstructing the network data signal data recovered from the output signal (Fig. 5, element 232, recovered clock counter , see column 6, lines 32-35, column 9, lines 4-21).

With respect to claim 14, all of the limitations of claim 14, are analyzed above in claim 13, and Cranford et. al., discloses: wherein the means for detecting erroneous performance by the transceiver further comprises a counter device for counting edge transitions of the network data signal within the established time window (see Fig. 5, element 228, column 6, lines 30-32, at the receiver side that detects the erroneous performance of the transceiver, see column 3, lines 43-48).

With respect to claim 15, claim 15 is analyzed similarly to claim 6 above.

With respect to claims 16, 17, these claims are analyzed similarly to claims 13-14 above.

Claims 18-20 are analyzed similarly to claims 15-17.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-4 , 6-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cranford Jr. et. al., (U.S. 6,298,458) in view of Drost et. al.,(U.S. 6,076,175).

With respect to claim 1, Cranford et. al., disclose: a transmitter for receiving a network data signal representative of a signal capable of being transmitted over a network and a control signal for impairing characteristics of the network data signal (Fig. 5, see "transmitter side of BIST", data signal 221, and combination of elements control logic 220, and counters 215a, 215b, see column 3, lines 32-43, column 5, lines 23-37) for continuously generating an output signal corresponding to the data signal and the control signal during a predetermined time window (see column 10, lines 4-9); a receiver for continuously receiving the output signal from the transmitter (Fig. 5, receive side of BIST, see column 3, lines 43-48), and for reconstructing the network data signal

within the predetermined time window (see column 10, lines 4-9); and a built-in-self-test (BIST) device for generating the network data signal and the control signal (Fig. 5, see column 3, lines 32-43), wherein the BIST device detects erroneous performance by the transceiver based on the reconstructed network data signal (column 3, lines 45-47).

Cranford et. al. do not expressly teach: a built-in-self-test (BIST) device for providing a clock signal with a varied offset for jitter testing the transceiver. In the same field of endeavor, Drost et. al., discloses a transmitter receiving a control signal for impairing characteristics of the network data signal and for continuously generating an output signal corresponding to the data signal and the control signal during a predetermined time window (Fig. 3 and Fig. 7, column 3, lines 18-33, column 5, lines 54-67, column 6, lines 1-5). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use the system of Drost et. al., to determine test the reliability of the chip (transceiver) i.e. determine the actual BER of the device (see column 1, lines 63-65, column 7, lines 11-29).

With respect to claim 2, all of the limitations of claim 2, are analyzed above in claim 1, and Cranford et. al. discloses: wherein the control signal includes signals for impairing a phase and an amplitude of the network data signal (see column 7, lines 65-67, column 8, lines 1-5, slurring control is understood to be relevant to an amplitude and phase impairment of the signal).

With respect to claim 3, all of the limitations of claim 3, are analyzed above in

claim 1, and Drost et. al., discloses: a jitter control system (Fig. 7, column 3, lines 26-28). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use jitter control system of Drost et. al., in the BIST of Cranford et. al., because the jitter control system (part of the BER evaluation system) allows for determination of an actual BER of chips i.e. the reliability of the chip (column 7, lines 11-20).

With respect to claim 4, all of the limitations of claim 4, are analyzed above in claim 3.

With respect to claim 6, all of the limitations of claim 6 are analyzed above in claim 1, and Cranford et. al., disclose: wherein the BIST device further comprises a pulse width counter for varying a pulse width of the network data signal (see column 5, lines 23-48, counters 215a and/or 215b , duty cycle (ratio of pulse duration over the period) corresponds to the pulse width).

With respect to claim 7, all of the limitations of claim 7 are analyzed above in claim 6, and Cranford et. al., disclose: wherein the pulse width counter tests a clock recovery capability of the receiver (column 5, lines 42-48 in understood that the pulse width counter is used to generate data that will test circuit responses, column 10, lines 12-17, where the recovered clock frequency may be compared to the expected clock frequency, i.e. the clock recovery capability of the receiver is tested).

With respect to claim 8, claim 8 is analyzed similarly to claim 1 above, and notice that Drost et. al. disclose: varying an offset of a clock signal embedded within the network data (see column 3, lines 18-26, 45-50, where the clock recovery operation at the receiver side from the data signal input, implies that the clock signal (with the varied offset) is embedded with the data at the receiver side).

With respect to claims 9, all of the limitations of claim 9, are analyzed above in claim 8, and Cranford et. al. discloses: wherein the control signal includes signals for impairing a phase and an amplitude of the network data signal (see column 7, lines 65-67, column 8, lines 1-5, slurring control is understood to be relevant to an amplitude and phase impairment of the signal).

With respect to claim 10, all of the limitations of claim 10 are analyzed above in claim 9, and Cranford et. al., disclose: wherein the BIST device comprises means for programming the network data signals (Fig.5, combination of counters 215a,215b and 220 control logic, as well as output signal 221 going to the protocol generator, see also column 4, lines 45-52 referring to the protocol generator in the transmitter side, and column 5, lines 26-27 i.e. the control logic allows programming of the network data).

With respect to claim 11, all of the limitations of claim 11, are analyzed above in claim 8, and Cranford et. al., disclose: wherein the transmitter and the receiver are provided on a single integrated circuit, the transceiver further comprising a transfer gate for selectively coupling the output signal from the transmitter to the receiver within the

integrated circuit (see Fig. 4, element 173, transfer gate).

With respect to claim 12, all of the limitations of claim 12 are analyzed above in claim 8, and Cranford et. al., discloses: wherein the network data signal includes an embedded clock signal, and wherein the BIST device comprises means for locking onto the embedded clock signal (see column 5, lines 58-62 , PLL clock recovery understood to recover an embedded clock signal from the received data signal).

With respect to claim 13, all of the limitations of claim 13 are analyzed above in claim 12 and Cranford et. al., disclose: wherein the means for detecting erroneous performance by the transceiver comprises a counter device for counting edge transitions of the clock signal for establishing a time window for reconstructing the network data signal data recovered from the output signal (Fig. 5, element 232, recovered clock counter , see column 6, lines 32-35, column 9, lines 4-21).

With respect to claim 14, all of the limitations of claim 14, are analyzed above in claim 13, and Cranford et. al., discloses: wherein the means for detecting erroneous performance by the transceiver further comprises a counter device for counting edge transitions of the network data signal within the established time window (see Fig. 5, element 228, column 6, lines 30-32, at the receiver side that detects the erroneous performance of the transceiver, see column 3, lines 43-48).

With respect to claim 15, claim 15 is analyzed similarly to claim 6 above.

With respect to claims 16, 17, these claims are analyzed similarly to claims 13-14 above.

Claims 18-20 are analyzed similarly to claims 15-17.

Allowable Subject Matter

6. Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Schneider (U.S. 6,201,829) discloses: a BIST for high speed transceiver testing.

Ramamurthy et. al., (U.S. 5,787,114) disclose: BIST for transceiver testing.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SOPHIA VLAHOS whose telephone number is 571 272 5507. The examiner can normally be reached on MTWRF 8:30-17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed Ghayour can be reached on 571 272 3021. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

7/31/2006
SV

MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER